WHAT IS CLAIMED IS:

1. A method for manufacturing an interconnect for an integrated circuit, comprising:

forming a surface conductive lead in an opening formed within a protective overcoat and over a barrier layer, a portion of the barrier layer extending beyond the surface conductive lead; and

subjecting the portion of the barrier layer to a dry etch to remove the portion, the dry etch selective to the barrier layer.

2. The method as recited in Claim 1 wherein the dry etch includes carbon tetrafluoride.

3. The method as recited in Claim 2 wherein the dry etch further includes nitrous oxide.

4. The method as recited in Claim 2 wherein the dry etch further includes oxygen or chlorine.

5. The method as recited in Claim 1 wherein the barrier layer is a tungsten titanium barrier layer.

6. The method as recited in Claim 1 wherein the barrier layer has a thickness ranging from about 200 nm to about 300 nm.

7. The method as recited in Claim 1 further including a seed layer located between the barrier layer and the surface conductive lead, and further including subjecting the seed layer to a wet etch prior to subjecting the portion of the barrier layer to the dry etch.

8. The method as recited in Claim 7 wherein the wet etch includes an etch chemistry including hydrogen peroxide and sulfuric acid.

9. The method as recited in Claim 1 wherein the surface conductive lead has a width ranging from about 3 μm to about 200 μm.

10. The method as recited in Claim 1 wherein the protective overcoat comprises one or more layers selected from the group consisting of silicon oxynitride layers, silicon oxide layers, and silicon nitride layers, phospho-silicate glass layers, and organic polymer layers.

11. An interconnect for use in an integrated circuit, comprising:

a surface conductive lead located in an opening formed within a protective overcoat; and

a barrier layer located between the protective overcoat and the surface conductive lead, a portion of the barrier layer forming a skirt that extends outside a footprint of the surface conductive lead.

12. The interconnect recited in Claim 11 wherein the skirt extends from about 250 nm to about 2000 nm outside the footprint.

13. The interconnect recited in Claim 11 wherein a thickness of the skirt tappers down as is moves away from the surface conductive lead.

14. The interconnect recited in Claim 11 further including a seed layer located between the barrier layer and the surface conductive lead, wherein substantially no undercut exists in the seed layer.

15. The interconnect recited in Claim 11 wherein the surface conductive lead has a width ranging from about 3 μm to about 200 μm.

16. A method for manufacturing an integrated circuit, comprising:

forming transistor devices over a semiconductor substrate;

forming one or more metallization layers over the transistor devices, the one or more metallization layers interconnecting one or more of the transistor devices;

forming a protective overcoat over the one or more metallization layers, wherein the protective overcoat has an opening located therein;

forming a surface conductive lead in the opening and over a barrier layer, a portion of the barrier layer extending beyond the surface conductive lead; and

subjecting the portion of the barrier layer to a dry etch to remove the portion, the dry etch selective to the barrier layer.

17. The method as recited in Claim 16 further including a seed layer located between the barrier layer and the surface conductive lead, and further including subjecting the seed layer to a wet etch prior to subjecting the portion of the barrier layer to the dry etch.

18. The method as recited in Claim 17 wherein the wet etch includes an etch chemistry including hydrogen peroxide and sulfuric acid.

19. The method as recited in Claim 16 wherein the surface conductive lead has a width ranging from about 3 μm to about 200 μm.

20. The method as recited in Claim 16 wherein the protective overcoat comprises one or more layers selected from the group consisting of silicon oxynitride layers, silicon oxide layers, and silicon nitride layers, phospho-silicate glass layers, and organic polymer layers.